REMARKS

Reconsideration of this application, as amended, is respectfully requested.

Claims 1-7, 9-18, 20-32 and 34-41 are pending. Claims 1-7, 9-18, 20-32 and 34-41 have been rejected. Claim 25 has been objected to.

Claims 1, 12, 23, 25, and 26 have been amended. No claims have been canceled. No claims have been added. Support for the amendments is found in the specification, the drawings, and in the claims as originally filed. Applicants submit that the amendments do not add new matter.

Applicants reserve all rights with respect to the applicability of the Doctrine of Equivalents.

The Examiner objected to claim 25 because of informalities.

Applicants have amended claim in light of the Examiner's objection.

Therefore, applicants submit that the Examiner's objection with respect to claim 25 has been overcome.

The Examiner rejected claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,282,556 to Chehrazi et al. ("Chehrazi") in view of U.S. Patent No. 6,036,350 to Mennemeier et al. ("Mennemeier").

Amended claim 1 reads as follows:

> A method for execution by a microprocessor in response to receiving a single instruction, the method comprising:
>
> receiving a first vector of numbers from a first entry in a register file and a second vector of numbers from a second entry in the register file;
>
> selecting a first plurality of numbers of the first vector from the first entry and a second plurality of numbers of the second vector from the second entry according to a configuration specified by the instruction; and
>
> generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers; wherein the

third plurality of numbers are saved in a third entry in the register file;
wherein the above operations are performed in response to the microprocessor receiving the single instruction.

(emphasis added)

It is respectfully submitted that none of the references cited by the Examiner teach or suggest a combination with each other. It would be impermissible hindsight, based on applicants' own disclosure, to combine the cited references.

More specifically, Chehrazi discloses:

... The SABD operation computes the differences between corresponding operands stored in the operand registers, Vt and Vs, under control of the format field, determines the absolute value of these differences then adds the absolute value differences together to arrive at a final sum. ....

(Chehrazi, col. 20, lines 47-52)(emphasis added)

In particular, Chehrazi discloses:

FIG. 20B is a diagram 570 that illustrates the operation of the SABD instruction in one exemplary mode. Input register 310 contains 16 separate 8-bit operands called 310(a)-310(p). Input register 312 contains 16 separate 8-bit operands called 312(a)-312(p). As shown in FIG. 20B, each separate operand of register 310 has a corresponding operand of register 312, e.g., operand 310(f) corresponds to operand 312(f), etc...

(Chehrazi, col. 20, line 61-col. 21, line 1)(emphasis added)

Thus, Chehrazi merely discloses a first input register (310) that stores a [vector] of operands Vt and a second input register (312) that stores a [vector] of operands Vs (Figure 20B). In contrast, amended claim 1 refers to receiving a first vector of numbers from a first entry in a register file and a second vector of numbers from a second entry in the same register file.

Further, Chehrazi merely discloses computing the differences between corresponding operands stored in the operand registers, Vt and Vs. In contrast, amended claim 1 refers to selecting a first plurality of numbers of the first vector from the first entry and a second plurality of numbers of the second vector from the second entry according to a configuration specified by the instruction.

Additionally, Chehrazi merely discloses a third destination register Vd that stores the sum of absolute differences of operands from the first and second registers. In contrast, amended

claim 1 refers to generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, wherein the third plurality of numbers are saved in a third entry in the register file.

Mennemeier, in contrast, discloses a method of sorting signed numbers and solving absolute differences using packed instructions (Abstract), and similarly to Chehrazi, fails to disclose the discussed limitations of amended claim1.

Further, even if a method of sorting signed numbers of Mennemeier were incorporated into the pipelined data path of Chehrazi, such a combination would still lack receiving a first vector of numbers from a first entry in a register file and a second vector of numbers from a second entry in the same register file, as recited in amended claim 1.

Furthermore, even if a method of sorting signed numbers of Mennemeier were incorporated into the pipelined data path of Chehrazi, such a combination would still lack selecting a first plurality of numbers of the first vector from the first entry and a second plurality of numbers of the second vector from the second entry according to a configuration specified by the instruction, as recited in amended claim 1.

Moreover, even if a method of sorting signed numbers of Mennemeier were incorporated into the pipelined data path of Chehrazi, such a combination would still lack generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, wherein the third plurality of numbers are saved in a third entry in the same register file, as recited in amended claim 1.

Therefore, applicants respectfully submit that amended claim 1 is not obvious under 35 U.S.C. § 103(a) over Chehrazi, in view of Mennemeier.

Given that claims 2-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 contain the limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claims 1-3, 5-7, 9-14, 16-18, 20-28, 30-32, 34-38, and 40-41 are not obvious under 35 U.S.C. § 103(a) over Chehrazi, in view of Mennemeier.

The Examiner rejected claims 4, 15, 29, and 39 under 35 U.S.C. § 103(a) as being unpatentable over Chehrazi in view of Mennemeier as applied to claims 1, 2, 12, 26, and 27 above, and further in view of European Patent Application No. EPO 0 485 776 A2 to Diefendorff et al. ("Diefendorff").

It is respectfully submitted that none of the references cited by the Examiner teach or suggest a combination with each other. It would be impermissible hindsight, based on applicants' own disclosure, to combine the cited references.

Diefendorff, in contrast, discloses a method for executing graphics pixel packing instructions in a data processor.

Furthermore, even if a method of sorting signed numbers of Mennemeier and a method for executing graphics pixel packing instruction of Diefendorff were incorporated into the pipelined data path of Chehrazi, such a combination would still lack receiving a first vector of numbers from a first entry in a register file and a second vector of numbers from a second entry in the same register file, as recited in amended claim 1.

Furthermore, even if a method of sorting signed numbers of Mennemeier and a method for executing graphics pixel packing instruction of Diefendorff were incorporated into the pipelined data path of Chehrazi, such a combination would still lack selecting a first plurality of numbers of the first vector from the first entry and a second plurality of numbers of the second vector from the second entry according to a configuration specified by the instruction, as recited in amended claim 1.

Moreover, even if a method of sorting signed numbers of Mennemeier and a method for executing graphics pixel packing instruction of Diefendorff were incorporated into the pipelined data path of Chehrazi, such a combination would still lack generating simultaneously a third plurality of numbers, each of which is an absolute difference between a number in the first plurality of numbers and a number in the second plurality of numbers, wherein the third plurality of numbers are saved in a third entry in the same register file, as recited in amended claim 1.

Given that claims 4, 15, 29, and 39 contain the limitations that are similar to those discussed with respect to amended claim 1, applicants respectfully submit that claims 4, 15, 29, and 39 are not obvious under 35 U.S.C. § 103(a) over Chehrazi, in view of Mennemeier, and further in view of Diefendorff.

It is respectfully submitted that in view of the amendments and arguments set forth herein, the applicable rejections and objections have been overcome. If there are any additional charges, please charge Deposit Account No. 02-2666 for any fee deficiency that may be due.

Respectfully submitted,

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